An Introduction to Semiconductor Detectors

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Definition

A solid state (silicon) detector is an ionization chamber
- Sensitive volume with electric field
- Energy deposited creates e-h pairs
- Charge drifts under E field
- Get integrated by ROC
- Then digitized
- And finally is read-out and stored

Buffering and discriminations stages can be implemented
Outline

- Particle detection
- Principle of operation of solid state devices
  - The p-n junction
- Processing
- Detector design
- Performance
- Radiation Damage
- Electronics and readout
- Assembling Detectors
- Trends
  - Rad hard sensors
  - Highly segmented detectors
  - Large detectors
**Particle Detection**

- **HEP detectors aim at:**
  - Coverage of full solid angle
  - Measure momentum and energy \((E,p)\)
  - Identify particles (mass, charge)
  - Precisely measure decay vertices
  - Fast response ⇒ no deadtime

- **Particles are detected via their interaction with matter**
  - Different physical processes
  - For charged particles predominantly excitation and ionization

- **Trackers (p) and vertex detectors**
  - Thin (low-Z) material (gas, liquid or solid)

- **Calorimeter (E)**
  - High-Z material (absorber)

Chris Fabian
Multipurpose Physics Detectors

- Tracking detector
- Magnetic coil
- Hadron calorimeter
- EM calorimeter
- Muon Chambers

Particles:
- Photons
- Electrons
- Quarks => Jets
- Muons
Tracking and vertex detectors were crucial to the discovery of top: \( pp \rightarrow t\bar{t} \rightarrow WbWb \rightarrow \ell\nu\ell\nu bb \). Vertex detection will be even more important for searches of Higgs and SUSY at the LHC.
Solid State Detectors (SSD)

Ionization chamber medium could be gas, liquid, or solid
- Gas \(\Rightarrow\) electron and ion pairs; Semiconductor \(\Rightarrow\) electron and hole pairs

<table>
<thead>
<tr>
<th></th>
<th>Gas</th>
<th>Solid</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Atomic number (Z)</td>
<td>Low</td>
<td>Moderate (Z=14)</td>
</tr>
<tr>
<td>Ionization Energy (\varepsilon_1)</td>
<td>Moderate ((\approx) 30 eV)</td>
<td>Low ((\approx) 3.6 eV)</td>
</tr>
<tr>
<td>Signal Speed</td>
<td>Moderate (10ns-10(\mu)s)</td>
<td>Fast (&lt;20 ns)</td>
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</tbody>
</table>

Solid State Detectors
- Energy (E) to create e-h pairs 10 times smaller than gas ionization \(\Rightarrow\) increase charge \(\Rightarrow\) good E resolution
- \(\frac{\Delta E}{E} \propto \frac{1}{\sqrt{N}} \propto \frac{1}{\sqrt{E/\varepsilon_1}} \propto \sqrt{\varepsilon_1}\)
- Greater density
  - Reduced range of secondary electron \(\Rightarrow\) excellent spatial resolution
  - Average \(E_{loss}\) \(\approx\) 390eV/ \(\mu\)m \(\approx\) 108 e-h/ \(\mu\)m (charge collected is a function of thickness D but no multiplication)
- To minimize multiple scattering D should be small, 300 \(\mu\)m \(\approx\) 32,000 e-h pairs yields good S/N
Semiconductor crystals

- Most semiconductors have Zincblende and Diamond Structure
- Each atom is surrounded by 4 equidistant nearest neighbors which lie at the corner of a tetrahedron
- [semiconductor cell animation]

Lattice constant $a$
- Diamond: 3.56 Å
- Ge : 5.65 Å
- Si : 5.43 Å
Semiconductor: Band Gap

- When isolated atoms are brought together to form a lattice, the discrete atomic states shift to form energy bands.

- If the gap is large, the solid is an insulator. If there is no gap, it is a conductor. A semiconductor results when the gap is small.

  - Ge 0.7 eV
  - GaAs 1.4 eV
  - Si 1.1 eV
  - Diamond 4.5 eV
Silicon

- Excellent detector material
  - Low ionization energy (good signal). The band gap is 1.1 eV, but it takes 3.6 eV to ionize an atom. The rest of the energy goes to phonon excitations (heat).
  - Long mean free path (good charge collection efficiency)
  - High mobility (fast charge collection)
  - Low Z (Z=14 low multiple scattering)
- Oxide (SiO$_2$) has excellent electrical properties
- Good mechanical properties
  - Easily patterned to small dimensions
  - Can be operated in air and at room temperature (many SSD require cooling)
- Industrial experience and commercial applications
- Crystalline $\Rightarrow$ radiation damage

Principle of Operation

- Goal: precise charged particle position measurement
- Use ionization signal (dE/dx) from charged particle passage

- In a semiconductor, ionization produces electron hole (e-h) pairs
- Use an electric field to drift the e and h to oppositely charged electrodes

- Problem: in pure intrinsic (undoped) silicon, there are more free charge carriers than those produced by a charged particle.
  Ex.: in this volume have $4.5 \times 10^8$ free charge carriers and only $3.2 \times 10^4$ produced by MIP particle

- Problem: electron–hole pairs quickly re-combine
- Solution: Deplete the free charge carriers and collect e (or h) quickly by exploiting the properties of a p-n junction (diode)
What Are Diodes Made Out Of?

- Silicon (group 4). Each atom shares 4 valence electrons with its four closest neighbors through covalent bonds.
- The valence band will have 8 electrons.
- At $t=0K$ all electrons are in valence band and the conduction band is empty.
- As $T$ increases some electrons will jump the gap to the conduction gap
  - Pure Si: intrinsic carrier concentration $n_i \approx 10^{10}$ cm$^{-3}$ at 300K, Lattice $\approx 5 \cdot 10^{22}$ atoms/cm$^{-3}$ implies many states are available for carrier motion.

- The probability that an energy state is occupied by an electron is given by the Fermi-Dirac distribution:

$$f = \frac{1}{1 + e^{\frac{E-E_F}{kT}}}$$

- Where $E_F$ is at midgap for intrinsic silicon.
In an n-type semiconductor, electron carriers are obtained by adding an atom with 5 valence electrons: arsenic, antimony, and phosphorus.

- Electrons are the majority carriers.
- Donors introduce energy levels 0.01 eV below the conduction band ⇒ Fermi Level moves close to CB.

The 2D diagram shows the extra electron in n-type materials.

This extra electron is loosely bound.

\[ E_i(\text{lattice}) = \frac{E_i(\text{atom})}{\varepsilon_{Si}^2} \]
In a p-type semiconductor, holes carriers are obtained by adding impurities of acceptor ions like Boron (type III in the periodic table).

- **Holes are the majority carriers.**
- Acceptors introduce energy levels close to valence band and thus ‘absorb’ electrons from VB, creating holes. Fermi Level moves close to VB.

- The 2D diagram shows the extra hole in p-type materials.
- This extra hole is loosely bound.
Space Charge Region: When n and p type silicon are brought together → gradient of electron and hole densities → migration of majority carriers across the junction which leaves a region of net charge of opposite sign on each side, called the space-charge region or depletion region (depleted of free charge carriers). The electric field in the region prevents further migration of carriers → potential difference $\Phi = V_{bi}$ (built in potential).

Junction: Interface where the p- and n-type materials meet.

$N_A$ & $N_D$: Negative and positive doping (n/cm$^3$), usually $\approx 10^{15} - 10^{20}$/cm$^3$.

p-n e-field
The pn junction is considered biased when an external voltage is applied. There are two types of biasing: Forward bias and Reverse bias. biased p-n junction
pn-Junction Overview

- p-type and n-type doped silicon forms a region depleted of free charge carriers
- The depleted region contains a non-zero fixed charge and an electric field. In the depletion zone, electron – hole pairs do not recombine but drift along field lines
- The depletion region can be increased by applying a reversed bias voltage ⇒ allows charge collection from a larger volume
Depletion region

Depletion depths for an abrupt p-n junction are found by solving Poisson eq. Note that charge conservation implies that $N_A d_p = N_D d_n$

$$d_p = \sqrt{\frac{2\varepsilon V_{bias}}{q} \frac{1}{N_A(1 + N_A / N_D)}}$$

$$d_n = \sqrt{\frac{2\varepsilon V_{bias}}{q} \frac{1}{N_D(1 + N_D / N_A)}}$$

If $N_D >> N_A$ then the depletion region is wide on the n-side and shallow on the p-side (Ex. $N_A = 10^{15}\text{cm}^{-3}$, $N_D = 5\cdot10^{12}\text{cm}^{-3}$, $d_p = 0.4 \mu\text{m}$ and $d_n = 300 \mu\text{m}$ at $V_{bias} = 100\text{ V}$)

$$d = \sqrt{\frac{2\varepsilon V_{bias}}{q} \frac{1}{N_D}} \quad \text{if} \quad N_A >> N_D$$

The voltage needed to deplete the silicon thickness $D$ is called the full depletion voltage $V_{fd}$. The E field is given by

$$E(x) = \frac{2V_{fd}}{D} \left(1 - \frac{x}{D}\right) + \frac{V_{bias} - V_{fd}}{D}$$
Depletion Zone: Properties

The resistivity of the silicon depends on:
- the electron, hole mobility: \( \mu_e, \mu_h \)
- the densities of electron and holes \( n \) and \( p \). If \( N_A, N_D >> n_i \) then \( n = N_D - N_A, p = N_A - N_D \)

\[
\rho = \left( \frac{1}{q(\mu_e n + \mu_h p)} \right)
\]

If \( N_D >> N_A \) or vice versa then \( \rho = 1/(q\mu N) \) and \( d \) can be written in terms of \( \rho, \mu \) and \( V_{bias} \):

\[
d = \sqrt{\frac{2\varepsilon \rho \mu V_{bias}}{}}
\]

and \( V_{fd} \)

\[
V_{fd} = \frac{D^2}{(2\varepsilon \rho \mu)}
\]

Higher voltage is needed to fully deplete a low resistivity material.

Higher voltage is needed to deplete p-type bulk since the carrier mobility of holes is lower than for electrons (450 vs 1350 cm²/V·s)
The depletion voltage can be determined by measuring the capacitance versus reverse bias voltage. The capacitance is simply the parallel plate capacity of the depletion zone.

\[ \frac{1}{C^2} \text{ vs voltage} \]

\[ 1/C^2 \text{ vs voltage} \]

\[ V_{fd} \]
Diode I-V curve

- $V_B = \text{Bias Voltage}$
- $I_D = \text{Current through Diode. } I_D \text{ is Negative for Reverse Bias and Positive for Forward Bias}$
- $I_S = \text{Saturation Current (leakage current)}$
- $V_{BR} = \text{Breakdown Voltage}$
- $V_\phi = \text{Barrier Potential Voltage which correspond the “built-in” voltage}$

$$V_{bi} = \frac{kT}{q} \ln \frac{N_D N_A}{n_i^2}$$
Leakage Current

The current in a reversed-biased diode is due to thermally generated minority carriers that can not recombine because of E field:

- Diffusion current: charge generated in the undepleted zone adjacent to the depletion zone which diffuse into the depletion zone
- Generation current $J_g$, charge generated in the depletion zone by defects or contaminants

$$J_g = \frac{1}{2} q \frac{n_i}{\tau_0} d$$

The intrinsic carrier density increases with temperature $\Rightarrow I_{\text{leak}}$ increases by a factor of 2 with a temperature increase of 8K

$I_{\text{leak}}$ sensitive to process quality
Charge collection

Electron and hole pairs created in the depletion region move under the E field

\[ v_{e,h}(x) = \mu_{e,h} E(x) \]

\[ \mu_e = 1500 \text{ cm}^2 / V\text{s}, \mu_h = 450 \text{ cm}^2 / V\text{s} \]

The time required for a carrier to traverse the sensitive volume is the collection time.

The collection time can be reduced by over-biasing the sensor

\[ t(x) = \frac{D^2}{2\mu_p V_d} \ln \left( \frac{V_{bias} - V_{fd}}{V_{bias} - V_{fd} + 2V_{fd}\left(1 - \frac{x}{D}\right)} \right) \]
1) Start with very pure quartzite sand. Clean it and further purify by chemical processes. Melt it and add the tiny concentration of phosphorus (boron) dopant to make n(p) type silicon. Pour it in a mold to make a polycrystalline silicon cylinder.

2) Using a single silicon crystal seed, melt the vertically oriented polysilicon cylinder onto the seed using RF power to obtain single crystal 'ingot'.

3) Slice ingot into wafers of thickness 300-500µm with diamond encrusted wire or disc saws.
Diode Processing

Start with n-doped silicon wafer, \( \rho \approx 1-10 \, \text{k}\Omega \text{cm} \). Silicon can be turned into n-type by neutron doping (\( ^{30}\text{Si} + n \rightarrow ^{31}\text{Si} \), \(^{31}\text{Si} \rightarrow ^{31}\text{P} + \beta^- + \nu \))

Oxidation at 800 - 1200°C

Photolithography (= mask align + photo-resist layer + developing) followed by etching to make windows in oxide
Diode Processing

4) Doping by ion implantation (or by diffusion)

5) Annealing (healing of crystal lattice) at 600 °C

6) Photolithography followed by Al metallization over implanted strips and over backplane usually by evaporation.

⇒ Simple DC-coupled silicon strip detector
Detectors: single sided devices

- Make several p-n junctions at the surface of a silicon n-type.
- Example low $N_D$ on one side and high $N_A$ on the other: $p^+\!-\!n$ junction
  - if $N_A \approx 10^{15} \text{ cm}^{-3}$ and $N_D \approx 5 \cdot 10^{12} \text{ cm}^{-3}$ then $d_p = 0.4 \ \mu\text{m}$ and $d_n = 300 \ \mu\text{m}$ for $V_{\text{bias}} = 100 \ \text{V}$. The n-type silicon is the ionization volume, p-type is needed to deplete.
- Metal creates good ohmic contact to p-type silicon. Good contact to n-type silicon can be achieved only with high concentration of donor atoms ($N_D > 10^{19}/\text{cm}^3$).
Bias Resistor and AC Coupling

- Need to collect/measure charge on each strip ⇒ high impedance bias connection (≈1 MΩ resistor) to isolate strips
- Couple input amplifier through a capacitor (AC coupling) to avoid large DC input from leakage current.

These structures are often integrated on the silicon sensor.
- Bias resistors: deposition of doped polycrystalline silicon
- Coupling capacitors: metal readout lines over the implants are separated by an insulating dielectric layer (SiO₂, Si₃N₄).

• Nice integration
• More masks
• Pin holes
Detectors: single sided devices

- Detector design is usually made mask by mask (layer by layer) using CADENCE
The Charge Signal

**Collected charge usually given for Minimum Ionizing Particle (MIP)**

- \( \frac{dE}{dx} \) \( Si = 3.88 \) MeV/cm
  - 300 \( \mu \)m thick \( \Rightarrow \) 116 keV mean energy loss
- For silicon detectors we often use the most probable loss (0.7 \( \times \) mean) \( \Rightarrow \) 81 keV
- Since 3.6 eV needed to make an e-h pair
  - 72 e-h/\( \mu \)m most probable energy loss
  - 108 e-h/\( \mu \)m average energy loss
- Most probable charge \( \approx 22500 \) e (=3.6 fC)

**Most probable charge \( \approx 0.7 \times \) mean**

**Mean charge**

---

**Measured Landau distribution in a 300 \( \mu \)m thick Si detector (Wood et al., Univ. Oklahoma)**
Landau distribution has a low energy tail which broadens because of noise.

- Noise sources:
  - Capacitance
    \[ \text{ENC} \propto C_d \]
  - Leakage Current
    \[ \text{ENC} \propto \sqrt{I} \]
  - Thermal Noise
    \[ \text{ENC} \propto \sqrt{kT/R} \]

Silicon sensors have low occupancy $\Rightarrow$ most channels have no signal. Good hits are select by requiring $N_{\text{ADC}} >$ noise tail. If cut is too high $\Rightarrow$ efficiency loss.

**Figure of Merit:** Signal-to-Noise Ratio $S/N$.

Drift velocity of charge carriers is \( v = \mu E \), so drift time, \( t_d = \frac{d}{v} = \frac{d}{\mu E} \)

- Typical values:
  \[
  d = 300 \ \mu \text{m}, \ E = 2.5 \text{kV/cm}, \ \mu_e = 1350 \ \text{cm}^2 / \text{V} \cdot \text{s}, \ \mu_h = 450 \ \text{cm}^2 / \text{V} \cdot \text{s}, \text{ so } t_d(e) = 9 \text{ns}, t_d(h) = 27 \text{ns}
  \]

During the drift, e and h diffuse by multiple collisions. The distribution follows a Gaussian with \( \sigma \):

\[
\sigma = \sqrt{2D t_d} \quad \text{D} = \frac{\mu kT}{q}
\]

Typical charge radius: \( \sigma \approx 6 \mu \text{m} \)

Charge Radius determines:
- resolution
- ‘Charge Sharing’, i.e. deposition of charge on several strips.
Double Sided Detectors

Why not get a 2nd coordinate by measuring the position of the (electron) charge collected on the opposite face?

Problem:
- n-strips are not isolated because of an electron accumulation layer at the Si-SiO₂ interface. This effect is due to the presence of positive charge in SiO₂ layer which attracts electrons.

SOLUTION
- p-strips in between the n-strips.
- Put "field plates" (metal over oxide) over the n-strips and apply a potential on the plates to repel the electrons.
Oxide Charge

- Many defects can appear at the interface between Si and SiO₂.
  - Some of the interface atoms will miss oxygen atoms and create Si-O bonds
  - Impurities (H, OH,N)
- These will create levels that can trap mobile electrons and holes (Interface traps)
- The charge due to the trapped electrons and holes onto the oxide defects is the “oxide charge”
- The oxide charge is usually positive \(\Rightarrow\) electron accumulation layer
- It can affect device characteristics: breakdown voltage, strip isolation, interstrip capacitance

![Diagram of oxide-silicon interface and associated defects](image-url)

**Figure 2.14** Illustration of the oxide–silicon interface and the associated defects: (a) a two-dimensional chemical-bond model and (b) the energy-band model.
Guard Rings

We have treated the silicon strip device as having infinite area, but it has edges. What happens at the edges?

- There is a voltage drop between biasing ring and edge (since top edge is at backplane voltage).
- n-type implants are put around the edge of the device at a proper distance between p bias ring and edge ring.
  - One or more “guard” rings (often left floating) are used to assure a gradual potential drop over this region.
  - Defects or oxide charge build-up in this region could lead to additional leakage current contributions (called guard current)
Avalanche Breakdown

- If one increases the bias voltage, eventually the field is high enough to initiate avalanche multiplication.
- This usually occurs around 30V/\(\mu\)m (compared to a typical operating field of <1V/\(\mu\)m).
- Local defects and inhomogeneities could result in fields approaching the breakdown point.

These effects can be reduced by careful design of the guard area.
Breakdown and Guard rings

Operation of silicon sensors at high depletion voltage without breakdown can be achieved using multiple guard rings.

6 Guard Ring Diodes

11 Guard Ring Diodes

D1G7/E4 Guards Potential
Bringing It All Together

Connectivity technology: some of the possibilities

- **High density interconnects (HDI):** Industry standard and custom cables, usually flexible kapton/copper with miniature connectors.

- **Soldering:** Still standard for surface mount components, packaged chips and some cables. Conductive adhesives are often a viable low temperature alternative, especially for delicate substrates.

- **Wire bonding:** The standard method for connecting sensors to each other and to the front-end chips. Usually employed for all connections of the front-end chips and bare die ASICs. A “mature” technology (has been around for about 40 years).

![OPAL (LEP) module with wiring diagram]

- ~200 wire bonds
- 4 x 640 wire bonds
- Total ~2700 wire bonds
Wire Bonding

- Ultrasonic power is used to vibrate needle-like tool on top of Al wire. Friction welds wire to metallized substrate underneath.
- Pitch: 80µm pitch in a single row and 40µm in two staggered rows (typical FE chip pitch is ≈44µm).
- ≈25µm diameter aluminum wire and bond to aluminum pads (chips) or gold pads (hybrid substrates).
- Used in industry (PC processors) but not with such thin wire or small pitch.

Electron micrograph of bond “foot”

View through microscope of wire bonds connecting sensor to fan-out circuit
Mechanical assembly

- Mechanical support
  - Alignment of assemblies w.r.t. support structure
    - 2-20 µm depending on requirements
  - Maintenance of alignment and fiducials
- Support of silicon
  - Detector can bow ~100µm
- Cooling of readout electronics
- High thermal conductivity low mass material: Be, BeO, graphite, carbon fiber...
- Access for wirebonding
Layer 3, at a radial distance of 7 cm from the IP, consists of 126 silicon wafers in eighteen ladders attached to 36,792 channels of readout electronics. Layer 4, at a radial distance of 10 cm from the IP, consists of 260 silicon wafers in 126 ladders attached to 53,144 channels of readout electronics. At the time of shipping, 23 of 26 ladders were mounted and tested. The final 3 layer 4 ladders are in process and will be added in future.

CLEO III detector, Purdue
The average loss is higher than the most probable one because of high energy electrons. These electrons can release additional electrons which drift perpendicularly to the track and yield measurement errors of several $\mu$m.
Spatial resolution

- Drift and diffusion also spoil position resolution.
- One can minimize this effect by optimizing the bias voltage
  - At lower voltages the resolution is worst because the detector is not fully depleted
  - At higher voltages one can reduce the drift time and diffusion
- Compromise with breakdown problems
- Saturation of the drift velocity

Resolution vs. $V_{Bias}$ [V]
Strip pitch and readout pitch

- Standard readout pitch for strip detectors is about 50 µm (smallest 20 µm).
- Since charge distribution has width less than 10 µm we expect most of the charge to be collected by one strip.
- For events that have signal on two strips, the position resolution improves.

\[ \eta = \frac{PH_R}{PH_L + PH_R} \]

- Single strip (\(\sigma=3.5\ \mu m\))
- Double strip (\(\sigma=2.3\ \mu m\))

We can increase the probability of having two hits with intermediate strips.
Silicon Readout

Silicon as a sensor
- 300 µm thick wafer
- High resistivity, purity
- Surface strips or other patterns

Silicon as readout
- Poor quality wafer
- Photolithography makes integrated circuits
- All structures contains in a few micron thickness
- Most important is transistor
- Current technology is CMOS 0.35 micron
Silicon Readout

- Detector readout relies on low noise electronics.
- Typical ROC front-end
  - $C_d$, $R_b$, $C_c$ are the sensors capacitance to ground, the bias resistance and the coupling capacitance.
  - $R_s$ is the series resistance on the input signal path

Amplifier $\Rightarrow$
  - Gain
    \[ A_Q \approx \frac{1}{C_f} \]

Pulse shaper $\Rightarrow$
  - Maximize S/N
  - Limits pulse to accommodate pulse rate
CMOS preamp

- Microplex chip, low noise compact preamplifiers can be fabricated using standard CMOS processes:
  - Small amplifier pitches
  - Low noise
  - Radiation hard processes available

Basic equations

\[
\tau = R_p C_p
\]

\[
g_m = \frac{\partial I_d}{\partial V_g}
\]

- Transductance

\[
A_o = g_m R_p
\]

- Open Loop gain

\[
Gain = \frac{1}{C_f}
\]

- Volts/Coulomb

\[
\tau_{in} = \frac{\tau}{A_o C_f}
\]
Silicon Readout

The equivalent circuit for noise analysis includes both current and voltage noise terms:

- **Shot noise**: fluctuation due to electron emission statistics \( \propto I_{\text{leak}} \)
- **Thermal noise due to velocity fluctuations of the charge carriers**:
  - \( \propto R_s \)
  - \( \propto 1/R_b \)
- **Amplifier noise 1/f spectrum**
- **Capacitive noise** \( \propto C_{\text{det}} \)
- Noise current flows through \( C_{\text{det}} \)
- Total noise is the integral over the bandwidth of the system

![Diagram of detector circuit with noise terms labeled](image)

![Graph showing noise charge vs. shaping time](image)
Amplifiers can be optimized for noise performance in specific applications

<table>
<thead>
<tr>
<th>Chip</th>
<th>t</th>
<th>Noise</th>
<th>Power</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Viking</td>
<td>1.5µs</td>
<td>135e+12e/pf</td>
<td>1.5 mW/ch</td>
<td>Long strips, slow response, e+,e-</td>
</tr>
<tr>
<td>SVXII/III</td>
<td>132 ns</td>
<td>490e+50e/pf</td>
<td>5mW/ch</td>
<td>Tevatron</td>
</tr>
<tr>
<td>APV</td>
<td>25ns</td>
<td>500e+30e/pf</td>
<td></td>
<td>LHC(CMS)</td>
</tr>
</tbody>
</table>
Events at the LHC

(+30 minimum bias events)

All charged tracks with pt > 2 GeV

Reconstructed tracks with pt > 25 GeV
Radiation Damage in Silicon

- Two general types of radiation damage
  - "Bulk" damage due to physical impact within the crystal
  - "Surface" damage in the oxide or Si/SiO$_2$ interface

- Cumulative effects
  - Increased leakage current (increased shot noise)
  - Silicon bulk type inversion (n-type to p-type)
  - Increased depletion voltage
  - Increased capacitance

- Sensors can fail from radiation damage
  - Noise too high to effectively operate
  - Depletion voltage too high to deplete
  - Loss of inter-strip isolation (charge spreading)

- Signal/noise ratio is the quantity to watch
Surface Damage

Surface damage generation:
- Ionizing radiation creates electron-hole pairs in the SiO$_2$
  - Many recombine, electrons migrate quickly
  - Holes slowly migrate to Si/SiO$_2$ interface since hole mobility is much lower than for electrons (20 cm$^2$/Vs vs. 2x10$^5$ cm$^2$/Vs)
  - Some holes ‘stick’ in the boundary layer

Surface damage results in
- Increased interface trapped charge
- Increased fixed oxide charges
- Surface generation centers

MOS devices are sensitive to surface damage
- Electron accumulation under the oxide interface can alter the depletion voltage (depends on oxide quality and sensor geometry)
- In silicon strip sensors, surface damage effects (oxide charge) saturate at a few hundred kRad
Surface Damage Effects

Charges in the oxide layer can cause:

- Risk to readout electronics
  - threshold shifts
  - noise and gain deterioration
- Increase in the sensors capacitances
- Single event upset in small feature size devices

Problems can be minimized by:

- Silicon crystal orientation (<100> rather than <111>) can minimize interface traps at boundary
- Reducing oxide thickness
  - Voltage shifts are proportional to the square of the thickness (0.25 µm CMOS more rad hard)
- Processing
Surface Damage

- Oxide charges in the silicon strip sensors depend on vendor
  - Oxide charge starts out high before irradiation
  - Adversely influences operation in certain biasing configurations
  - Could set a limit to max bias voltage
Process Defects and Scratches
Bulk Damage

- Bulk damage is mainly from hadrons displacing primary lattice atoms (for $E > 25 \text{ eV}$)
  - Results in silicon interstitial, vacancy, and large disordered region
  - 1 MeV neutron transfers 60-70 keV to recoiling silicon atom, which in turn displaces ~1000 additional atoms

- Defects can recombine or migrate through the lattice to form more complex and stable defects
  - Annealing can be beneficial
  - Defects can be stable or unstable
  - Displacement damage is directly related to the non-ionizing energy loss (NIEL) of the interaction
  - Varies by incident particle type and energy

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  - Varies by incident particle type and energy
Bulk Damage

- Displacement damage occurs for all particles
  - Pions and neutrons are typically the most numerous
- Particle flux in a collider environment
  - Experience from CDF Run I suggests $\Phi = \Phi_0/r^{1.7}$
  - Neutron flux falls less rapidly; it eventually becomes significant
- NIEL Radiation damage studies typically normalized to 1 MeV neutron damage equivalent

\[ \text{charged particle multiplicity} \]
Bulk Damage Effects

Leakage Current:
\[ \Delta I = \alpha(t)\Phi V \]
- \( \alpha(t) \) (damage constant), \( V \) (volume), and \( \Phi \) (fluence).
- Annealing reduces the current
- Independent of particle type

Depletion Voltage:
\[ V_{dep} = q|N_{eff}|d^2/2\varepsilon\varepsilon_0 \]
- Effective dopant concentration \( (N_{eff} = N_{donors} - N_{acceptors}) \), sensor thickness \( (d) \), permittivity \( (\varepsilon\varepsilon_0) \).
- Depletion voltage is parameterized in three parts:
  - Short term annealing \( (N_a) \)
  - A stable component \( (N_c) \)
  - Long term reverse annealing \( (N_\gamma) \)
Leakage Current

- Defects create intermediate states within the band gap
  - Intermediate states act as ‘stepping stones’ of thermal generation of electron/hole pairs
  - Some of these states anneal away; the bulk current reduces with time (and temperature) after irradiation

- Annealing function $\alpha(t)$
  - Parameterized by the sum of several exponentials $\alpha_i \exp(-t/\tau_i)$
  - Full annealing (for the example below) reached after ~1 year at 20ºC
  - At low temperatures, annealing effectively stops
  - Dependant on incident particle type (?)

![Classification of levels in the forbidden gap.](image)

$A$: shallow acceptor, e.g. $B$
$B$: deep donor, e.g. $C,O_i$
$C$: deep acceptor, e.g. $V O_i$
$D$: shallow donor, e.g. $P_i$
$E$: amphoteric level, e.g. $V V$

![Short-term current annealing for protons and neutrons following a short (26 min) irradiation.](image)
Leakage Current

- Measured values of $\alpha(t)$
  - One quotes measured values of $\alpha(t)$ after complete annealing at $T=20^\circ C$: $\alpha_{\infty} = \alpha(t=\infty)$
  - ‘World averages’ for $\alpha_{\infty}$ are:
    - $2.2 \times 10^{-17} \text{ A/cm}^3$ for protons, pions
    - $2.9 \times 10^{-17} \text{ A/cm}^3$ for neutrons
  - Recent results show $\alpha(t=80\text{ min}, T=60^\circ C) = 4.0 \times 10^{-17} \text{ A/cm}^3$ for all types of silicon, levels of impurities, and incident particle types (NIM A426 (1999)86).
Depletion Voltage

Depletion voltage is often parameterized in three parts (Hamburg model):

$$\Delta N_{\text{eff}}(T,t,\Phi) = N_A + N_C + N_Y$$

- **Short term annealing ($N_A$)**
  $$N_A = \Phi_{eq} \sum_i g_{a,i} \exp(-k_{a,i}(T)t)$$
  - Reduces $N_Y$ (beneficial)
  - Time constant is a few days at 20°C

- **Stable component ($N_C$)**
  $$N_C = N_{c0}(1-\exp(-c\Phi_{eq}))+g_C\Phi_{eq}$$
  - Does not anneal
  - Partial donor removal (exponential)
  - Creation of acceptor sites (linear)

- **Long term reverse annealing ($N_Y$)**
  $$N_Y = N_{Y,\infty}[1-1/(1+N_{Y,\infty}k_Y(T)t)], N_{Y,\infty} = g_Y\Phi_{eq}$$
  - Strong temperature dependence
  - 1 year at $T=20$°C or ~100 years at $T= -7$°C (LHC)
  - Must cool Si at the LHC
RD48 (Rose Collaboration) was formed at CERN to develop radiation hard sensors for the LHC
  - Introduce dopants to create radiation hard devices
  - Develop damage parameterization
Modifications to carbon and oxygen content are being used with success
  - O and C are the main impurities responsible for defect kinetics
  - Both react with vacancies and interstitials and form electrically active centers
  - Oxygen captures vacancies, reducing the number of $V_2O$, $di-$, or multi-vacancy complexes
RD50 is now looking at new materials for SLHC (10X radiation level of LHC)
Oxygen and Carbon content is set during ingot growth and is also altered by diffusion
- Standard high-purity float-zone processing (FZ) plus high temperature processing (~1100 C for > day)
- Diffusion-oxygenation during float-zone (DOFZ) processing is also possible

Oxygen-enrichment of FZ Silicon:
- Normal SiO₂ field oxide grown (~1000 C for 12 hours)
- Additional heating to 1200 C in N₂ (plot shows 6 hours vs 9 days)

Why not use the industry-standard CZ silicon?
- Low resistivity (100 Ωcm vs 2kΩcm)
- High carbon content (10^{17} cm⁻³)
Oxygenation Benefits

- Oxygen enhancement is beneficial:
  - Effective dopant concentration (depletion voltage) can be improved by up to a factor of 3
  - Saturation of the concentration of reverse annealing clusters; no longer proportional to $\Phi$
  - Longer time constant for reverse annealing

- Oxygenation only beneficial for charged radiation (larger number of vacancy-interstitial pairs)

- Under study:
  - Neutron irradiation
  - Optimal parameters for oxygenation
  - Why doesn’t oxygenated Si follow the NIEL hypothesis (more impurities is bad)?

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Fig. 18: Damage parameters $N_C$ for oxygenated and standard material as obtained from annealing experiments at 60°C after irradiation with 24 GeV/c protons.

Fig. 19: Damage parameters $N_Y$ for oxygenated and standard material as obtained from annealing experiments at 60°C after irradiation with 24 GeV/c protons.
Pixel sensors

- A solution to get precise 3-D information is to develop pixel sensors.
- Hybrid pixels

Fine pitch (50 µm) bump placements
Solder
Indium
CMS Pixel Sensors

- Baseline CMS design: $n^+\text{-}n$ pixels for partial depletion operation and increased Lorentz angle in high B field.
  - 78 $\mu$m $n^+$-implants. One open p-stops rings provide isolation and a resistive path for biasing.
  - Bump Pad $\approx$13 $\mu$m shifted by 25 $\mu$m for double column ROC.
Guard ring design

- **Requirements:**
  - Breakdown voltage > 300V (we do not see any breakdown in diodes up to 1000 V with 11 guard rings)
  - Read-out side grounded
  - Voltage drop on guards on the backside
P-stop design

- Prototypes have several p-stops options.
  - Verify performance after irradiation
  - Optimize the length and width of the resistive channel
  - Compare with standard p-stops

- F-Single open ring
- E-Step p-stop
- A-Double open ring
- Standard p-stops
Excellent production quality: all wafers have >80% good sensors
Average breakdown voltage around 600 V
No breakdown after irradiation to 1E15
Large Silicon Systems

CMS tracker (~2007)
- 12000 modules
- ~445 m² silicon area
- ~24,328 silicon wafers
- ~60 M readout channels

CDF SVX IIa (2001-)
- ~11m² silicon area
- ~750 000 readout channels
Moore’s Law: Exponential growth of sensitive area and number of electronic channels with time (doubling of IC integration capacity every 18 months)
Pioneering Silicon Strip Detectors

- **NA11 (CERN 1981)**
  - 24x36 mm$^2$ active area
  - 8 layers of silicon
  - 1m$^2$ readout electronics!

- **E706 (FNAL 1987)**
  - 50x50 mm$^2$ active area

Silicon sensor and readout electronics technology closely coupled with electronics miniaturization (transistors, ICs, ASICs ...) coming along, silicon detectors quickly took off ...

⇒ with electronics miniaturization (transistors, ICs, ASICs ...) coming along, silicon detectors quickly took off ...
CDF SVX IIa half-ladder: two silicon sensors with readout electronics (SVX3b analog readout chip) mounted on first sensor.

ATLAS SCT barrel module: four silicon sensors with center-tapped readout electronics (ABCD binary readout chip).
Large Silicon Detector Systems

POOF POOF POOF
LEP

POOF POOF POOF
Tevatron

POOF POOF POOF
LHC

POW!

Whoops...

P.Collins, ICHEP 2002
Conclusion

- Silicon has gone in a few decades from an exotic to a common tracking medium.
  - GLAST is using 80 m² silicon, CMS now proposes 164 m²
  - CMS will have > 5.5 million channels of silicon!
- Advances have been made in understanding and reducing radiation effects

“Solid-state detectors require high-technology devices built by specialists and appear as black boxes with unchangeable characteristics.”

- Tom Ferbel, 1987
References ....

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- Rainer Wallny
- Gino Bolla UTEV seminar:
  http://www.fnal.gov/orgs/utev/past_speakers.html
- R. Lipton Academic lectures: http://www-ppd.fnal.gov/eppoffice-w/Academic_Lectures/Past_Lectures.htm
- Steve Worm notes on Radiation Damage
- Animations from the Educational Java Applet (JAS) Service The applet resources are developed and maintained by Prof. C.R.Wie's group at SUNY at Buffalo: jas.eng.buffalo.edu
Silicon Readout

- To read out silicon sensors we use “charge-sensitive” amplifiers.
- Start with inverting voltage amplifier. The voltage gain is
  \[ \frac{dV_0}{dV_i} = -A \quad v_0 = -Av_i \]
  \[ v_f = (A + 1)v_i \]

- Ideally input impedance is \( \infty \) (i.e. no signal flows into the amplifier input)

- Connect feedback capacitor \( C_f \) between input and output.

\[ Q_f = C_f v_f = C_f (A + 1)v_i \]
\[ Q_i = Q_f \quad (Z_i = \infty) \]
\[ C_i = \frac{Q_i}{v_i} = C_f (A + 1) \]

\[ A_Q = \frac{dV_0}{dQ_i} = \frac{Av_i}{C_i v_i} = \frac{A}{C_i} = \frac{A}{A+1} \frac{1}{C_f} \approx \frac{1}{C_F} \]
Silicon Readout

- Some charge will remain on the detector $C_{\text{det}}$
- What fraction of the charge is measured:

$$\frac{Q_i}{Q_S} = \frac{C_i v_i}{Q_{\text{det}} + Q_i} = \frac{C_i}{Q_s} \frac{Q_s}{C_i + C_{\text{det}}} \approx \frac{1}{1 + \frac{C_{\text{det}}}{C_i}}$$

- Input coupling capacitor $>> C_i$ for high transfer efficiency

Diagram:
- Charges moving in detector induce change of charge on detector electrodes
- Detector capacitance discharges into amplifier
The Shockley Equation

• The transconductance curve is

\[ I_D = I_S(e^{V_D/\eta V_T} - 1) \]

• \( I_D \) is the current through the diode, \( I_S \) is the saturation current and \( V_D \) is the applied biasing voltage.

• \( V_T \) is the thermal equivalent voltage and is approximately 26 mV at room temperature. The equation to find \( V_T \) at various temperatures is:

\[ V_T = \frac{kT}{q} \]

\( k = 1.38 \times 10^{-23} \text{ J/K} \quad T = \text{temperature in Kelvin} \quad q = 1.6 \times 10^{-19} \text{ C} \)

• \( \eta \) is the emission coefficient for the diode. It is determined by the way the diode is constructed. It somewhat varies with diode current. For a silicon diode \( \eta \) is around 2 for low currents and goes down to about 1 at higher currents